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3-15-04 F/26154

NOTICE OF APPEAL FROM THE PRIMARY EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES (Large Entity)

Docket No. ITL.0227US

In Re Application Of: **Ronald K. Minemier**

Serial No.	Filing Date	Examiner	Group Art Unit
09/345,669	June 30, 1999	Eric D. Wisdahl	2615

Invention: **Sensing With Defective Cell Detection**

TO THE COMMISSIONER FOR PATENTS:

Applicant(s) hereby appeal(s) to the Board of Patent Appeals and Interferences from the decision of the Primary Examiner dated **December 16, 2003** finally rejecting Claim(s) **1-13 and 15-30.**

The fee for this Notice of Appeal is: **$330.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

Signature

Dated: **March 5, 2004**

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03/10/2004 TLUU11 00000059 09345669
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I certify that this document and fee is being deposited on **March 5, 2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Ronald K. Minemier	Art Unit:	2615
Serial No.:	09/345,669	Examiner:	Eric D. Wisdahl
Filed:	June 30, 1999		
For:	Sensing With Defective Cell Detection	Atty Docket:	ITL.0227US P7137

Commissioner for Patents
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APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed December 16, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

Claims 1-13 and 15-30 are rejected. Each rejection is appealed.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF THE INVENTION

Referring to FIG. 2, a digital portable PC camera 200 in accordance with one embodiment of the invention may include optics unit 202 to focus an optical image onto the focal plane of imager 204. Image data (e.g., frames) generated by imager 204 may be transferred to a random access memory (RAM) 206 (through memory controller 208) or flash memory 210 (through memory controller 212) via the bus 214. See specification at page 5, lines 6 through 23.

The camera 200 may also include a compression unit 216 that interacts with the imager 204 to compress the size of a generated frame before storing it in a camera memory (RAM 206 and/or flash memory 210). To transfer a frame of data to a computer, the camera 200 may include a serial bus interface 218 to couple the camera memory (RAM 206 and flash memory 210) to a serial bus 220.

The camera 200 may also include a processor 222 coupled to a bus 214 via a bus interface unit 224. In some embodiments, the processor 222 interacts with the imager 204 to adjust image capture parameters.

Referring to FIG. 3, the imager 204 may include a rectangular grid or array 300 of pixel sensors 302. This arrangement allows column and row decoders, 304 and 306 respectively, to selectively retrieve indications from the sensors 302.

Decoders 304 and 306 route the selected indications to a signal conditioning circuit 308 which may, among other functions, amplify and digitize the received signals. The signal conditioning circuit 308 may also furnish the resultant data signals to an output interface 310 which includes circuitry for interfacing the imager 204 to the bus 214. Control unit 312, through circuitry such as state machines and timers, may coordinate and control the scanning (e.g., selection by row and column decoders 306 and 308) of pixel sensor 302 indications, their subsequent processing by signal conditioning circuit 308, and their transmission to other elements of the camera 200 through an output interface 310. See specification at page 5, line 24, through page 7, line 5.

Camera operations may include normal image capture and calibration. During normal image capture, each pixel sensor 302 accumulates light energy from that portion of an image that is focused on it by optics 202 for a period of time referred to as the integration time or interval. At the expiration of the integration interval, pixel sensors 302 indicate the intensity of the received light energy by, for example, an analog voltage signal. Control circuit 312 routes the pixel sensor indications through column and row decoders 304 and 306 to the signal conditioning circuit 308 where they may be amplified and digitized to form a frame -- digital data signals representing the captured image. A frame may be compressed by compression unit 216 and transmitted to memory, and/or a computer system via the serial bus interface 218 and serial bus 220.

Referring to FIG. 6, defective pixels in the array 300 may be identified by using hardware and/or software flow 600. By analyzing the intensities of the output signals produced by each pixel given known illumination, one can determine whether the output signal produced by any given pixel is beyond the range of correct intensities values, thereby indicating that the pixel is

defective. Initially, the host computer 102 may configure the sensor for an exposure and frame size to be read out. Then, knowing the illumination conditions, a test limit range of high and low pixel values may be determined as indicated in block 602. Software or hardware counters which count the number of defects may be reset as indicated in block 604. Thereafter the image capture and pixel readout is initiated (block 606).

In the case of a software implementation, the software may be stored, for example, in the flash memory 210 for execution by the processor 222. Alternatively, the software may be stored in association with a processor that may be included as part of the output interface 310, as another example. See specification at page 8, line 20, through page 10, line 6.

As each pixel is readout, its intensity value is compared against the high and low test range values as indicated in block 608. The defect count is accumulated during readout. That is, each time a pixel intensity value is above the maximum or is below the minimum test range values, it is counted as a defect and accumulated in a software or hardware counter (block 610). After the readout is complete, the total count of defective pixels is compared to a quality goal, as indicated in block 612. If the quality goal is exceeded, the sensor may be deemed "defective" and may be discarded or otherwise identified as being of lower quality.

A hold-off signal 611 may be used to gate the defect counter from incrementing. This allows dummy, dark, reference, redundant or other non-desired column data to be excluded from the final defect count. The hold-off signal may be generated by the internal readout logic of the sensor and/or by a control bit in a control register in the sensor. This extra signal allows flexible testing of all parts of the array under a variety of illumination conditions, including complete darkness.

A hardware implementation of the flow illustrated in FIG. 6, shown in FIG. 7, may be implemented for example as part of the output interface 310 in one embodiment of the invention. A pair of multiplexers and magnitude comparators 700 and 716 may be used to check pixel values against pre-set ranges. The comparator 700 checks for the high test range violation and the comparator 716 may check for the low test range violation. Data from the signal conditioning circuit 308 may be provided along the data bus 711 to both the high limit check and low limit check comparators 700 and 716. The comparators may be full adders in one embodiment of the present invention. See specification at page 10, line 7, through page 11, line 14.

The magnitude comparators 700, 716 may form a window circuit. Any pixel value above or below a programmed threshold of the magnitude comparator 700, 716 results in a counting pulse from one of the comparators. The comparators have their trigger output lines logically tied together to generate a final count pulse for each color channel. Thus, each set of comparators 700 and 716 are coupled to an OR logic circuit 718 which in turn is coupled to a defect counter 720. The defect counter 720 is further controlled by a hold-off signal 719 as described previously.

The comparators 700 and 716 are coupled to a bank of registers 702, 704, 706, 708, 710 and 712 which have been programmed with high and low pixel values for the given illumination conditions. In other words, the host computer 102, in one embodiment of the present invention, may programmably set the values in the registers which serve as high and low violation levels for the comparators 700 and 716. A pair of registers are used for each color channel. Thus, in a conventional red, green, blue (RGB) system, six registers may be provided. In a system with two green planes (Green 1 and Green 2), separate or, as illustrated, combined registers may be

utilized for the pair of green color channels. The bit width the registers 702-712 may be determined by the analog to digital conversion width of the imaging sensor 108 itself.

The register values in the registers 702-712 may be multiplexed to the comparators 700 and 716. The digital counter 720 may be incremented based on whether either magnitude comparator 700, 716 for the channel in use has crossed its threshold. The counter 720 may be arranged to be readable through the system's parallel or serial interfaces. The width of the counter may be determined by production based test limits. The counter may also have an overflow bit to detect more massive defect conditions. Sequencing circuits in the registers 702-716 determine which set of register values are sent to the magnitude comparators 700, 716. See specification at page 11, line 15, through page 13, line 2.

A flow 800 for detecting columnar spatial defects, shown in FIG. 8, which may be implemented by software or hardware, begins by receiving a defective pixel indication as indicated at diamond 802. A defective pixel identification may come from the systems illustrated in FIGS. 6 and 7 for example. When a defective pixel is detected, its column address plus a programmable offset of that address are stored as a sum as indicated in block 804. During the remainder of the current row readout, the next defect detected (diamond 806) is compared to the previous defective column address plus the allowed spatial offset (block 808).

The programmable offset may be set by the computer system 102 based on considerations, such as the intended application or field of use of the image sensor, and the manufacturer's or sensor owner's quality standards. Thus, as indicated in diamond 806, upon detection of the next defective pixel in the same row, its column address is compared to the stored sum as indicated in block 808. If the column address of the new defective pixel is greater than the sum stored in block 804 (diamond 810), there is no spatial defect and the flow returns to

block 804 where the new address is added to the programmable offset to establish a new sum. At diamond 814, a check determines whether the end of the row has been reached. If not, the flow continues to recycle.

If the second defect has a spacing less than or equal to the programmable offset, as determined at diamond 810, then a software or hardware spatial defect counter may be incremented (block 812). If all the pixels in the row have not been read out (diamond 814), the second defective pixel's column address is then stored with the programmable offset (block 804). This process repeats itself across the full row as it is read out. See specification at page 13, line 3, through page 14, line 10.

When a new row is read out, the sum of the stored address and offset is cleared and a new row bit is set (block 816). The new row bit may be used to prevent previous column defects from affecting the count in a new row being readout. In addition, a hold-off signal 801 may also be used to further control the defect count as described previously.

Referring now to FIG. 9, a hardware implementation for the flow illustrated in FIG. 8 may be incorporated into a modified output interface circuit 310a. It may be included together with the circuitry illustrated in FIG. 7 in one embodiment of the present invention. A magnitude detector or comparator 902 adds the previous defective column address to the programmable offset value to form an exclusion address range. In one embodiment of the present invention, the detector 902 may be a full adder. An additional magnitude detector or comparator 908 may be used to subtract the next or current defective pixel column address from the sum of the previous defective column address plus the programmable offset value.

A programmable offset value is stored in the register 904 for the column spacing limit. The previous defective column address is latched in the register 906 and the current defective

column address may be latched in the register 910. The current defect address is received from the port 912 which may be coupled to the counter 720 of FIG. 7.

The output signal from the comparator 908 is coupled to a counter 914 which counts the columnar spatial defects. A register 916 holds a new row bit. The output signal from the counter 914 is provided to the processor 222 through an output port 918 coupled to the bus 214. See specification at page 14, line 11, through page 15, line 16.

When a defective pixel is detected, the column address plus the programmable offset are stored in the column address register 906. The next defect detected in the same row is compared to the previous defect column address plus the allowed offset. If the magnitude of the second defect's address is greater than the spatial offset, then the new address is latched in the register 906. If the second defect's address is less than or equal to the spatial offset, then the spatial defect count is incremented, and the second defect's column address is latched.

When a new row is read out, the address latch is cleared and a new row bit is set. This bit gates off the trigger line to the counter so that previous columnar defects do not affect the count of defects in the new row.

Referring next to FIG. 10, a flow 1000, which may be implemented in software or hardware, may be used to analyze row and column based spatial defects. The flow begins by globally resetting registers as indicated in block 1002. After the host computer has configured the sensor for an exposure and frame size to be read out, the host programs the "not allowed" row and column distance registers for the detected illumination conditions (block 1004). This sets the amount of spatial distance which will be detected as spatial row or column defects (block 1006).

As indicated in block 1008, the image capture is begun and the pixel values are readout. During the frame readout, the defective pixel detect circuits 310 detect defects and write their row and column addresses into a random access memory (RAM) array. The circuits 310 also set the defect exists bit in the RAM array as indicated in blocks 1010 and 1012. After the frame has been readout, a defect counter checks for an overflow condition (diamond 1014). That is, a determination is made as to whether the number of single point defects exceeds an allowed count. If so a defect overflow is indicated (block 1016). If the allowed single point defect is not zero and the overflow bit is not set, then the RAM array is checked to determine if any of the single point defects violate the spatial defect criteria for the sensor. See specification at page 15, line 17, through page 17, line 5.

Continuing in FIG. 11, a magnitude comparison may be used to detect defects. Each comparator subtracts a first row address against the second row address (block 1100). The resulting row address is subtracted from the proscribed spatial offset (block 1102). A spatial defect is indicated, if appropriate, in block 1104. A counter is used to log the individual defects. The same comparison is then done for the column addresses (diamond 1106).

The first defect address where a defect exists bit is set is accessed in the RAM array (block 1108). Then all other addresses are compared against the first address to detect spatial defects (block 1110). For RAM addresses where the defect exists bit is cleared, a signal may be generated to avoid counting any miscompares of either the row or column addresses. If a true spatial defect is detected in either a row or column, then a counter is caused to generate an event (block 1112). After the first address has been compared against all other addresses, then the next defect address may be stored and the compare and RAM array readout process is repeated (diamond 1114). This compare process may be repeated until all the addresses that have defect

exists bits are compared. When the full RAM array has been checked, the process stops and the user checks the counter contents to make the pass fail decision for the imaging sensor (block 1116).

Referring to FIG. 12, a RAM array 1202 may be provided in a modified output interface circuit 310b to store the row and column defect information. The depth of the array may be determined by the total single defect criteria for the device being tested. The width of the array may be determined by the full row and column address widths, plus one extra bit to signify that a location holds a defect. For example, if the total allowed single point defect count is 128, and the pixel array is 1024 columns by 1024 rows, then the RAM array may be 11 bits wide by 128 locations deep. See specification at page 17, line 6, through page 18, line 15.

A multiplexer 1206 reads the RAM array 1202 after frame readout has been concluded. Each RAM location with a valid defect may have its row and column addresses compared to all of the RAM locations that have an actual defect address stored in them. If enough pins exist on the die to be multiplexed and used as the address for the RAM array, then a tester can do the read sequencing of the RAM array. This saves the additional state machine logic to read out the RAM array. In this example, if a 10 bit analog to digital converter output port exists for the pixel, then after frame readout, these pins may be the entry point to the RAM array's 7 bit addressing.

A register 1216 stores the proscribed row and column distances that may constitute spatial defects, that is, whether there are two single point defects closer than X rows or Y columns apart. A latch 1212 holds the row and column address of the first defect location to be compared against all others. The latch 1212 is fed successive addresses by the multiplexer 1200

until all defect addresses have been compared by the comparators 1214 and 1218 against all other defect addresses.

A global reset in a hardware embodiment clears the defect exists bits in the RAM address array 1202. It may not be necessary to actually clear the RAM address locations as they may be ignored during later compare processes if the defected exists bit is not set. See specification at page 18, line 16, through page 19, line 16.

Two magnitude comparators 1214 and 1218 may detect defects and thereafter may be switched to act as magnitude comparators for the row and column addresses. Each comparator may be multiplexed a second time. The comparator 1214 subtracts the first row address from the second row address while the comparator 1218 subtracts the resulting row address difference from the proscribed distance and signals a spatial defect output signal as appropriate. The comparators are then switched to do the same process on the column addresses. The counter 1220 used to log individual defects in the embodiment of FIG. 7 may now be used to log spatial defects.

The first defect address where the defect exists bit is set may be latched and then all other addresses may be compared against the first address. The sequencing of data from the RAM array through the multiplexer 1206 and from the register 1216 is controlled by the multiplexer controller 1210 and the address decoder 1204. The defect exists bit may be separately read out through the multiplexer 1208 and passed directly to the comparator 1218. For RAM addresses where the defect exists bit is cleared, a hold off signal may be fed by a circuit 1222 to the trigger circuit of the counter 1220 to prevent any miscompares of either the row or column addresses.

If a true spatial defect is detected, in either a row or a column, then a trigger to the counter 1220 is generated. After the first address has been compared against all other addresses,

the next defect address is loaded into the defect address latch 1212 and then the compare and RAM array readout processes are repeated. This compare process is repeated until all addresses that have defect exists bits are compared. The address decoder 1204 to the RAM array may be arranged to simply rollover so that it always checks all locations regardless of what address on the RAM array is being checked against all other addresses. After the full RAM array has been checked, the process stops and the user checks the counter contents to make the proper pass/fail decisions. See specification at page 19, line 17, through page 21, line 2.

By detecting defective pixels in known programmable row and column spatial relationships in the image sensor itself during the sensor's normal capture frame readout process, the test system may be relieved of capturing a frame and then algorithmically determining spatial relationships. Thus, embodiments of the present invention save manufacturing cost by reducing memory needed to hold the captured frame, allowing inexpensive testers to be used. Manufacturing costs may be further reduced in some embodiments of the present invention by eliminating algorithmic processing time compared to saving the data to an array in the tester and then determining which pixels are spatially defective.

In one embodiment of the present invention, the defect detection circuits may be located on the same die as the imaging sensor. In other embodiments, they may be located on different die all in the same focal plane. See specification at page 21, line 3, through page 22, line 9.

VI. ISSUES

A. Is Claim 1 Anticipated by Kameyama?

B. Is Claim 1 Anticipated by Vincent?

C. Is Claim 6 Anticipated by Kameyama?

D. Is Claim 15 Anticipated by Vincent or Kameyama or Obvious Over the Combination of Vincent and Kameyama?

VII. GROUPING OF THE CLAIMS

Claim 1 may be grouped with claims 7-13, 22, and 24-30.

Claims 6, 29, and 30 may be grouped; and

Claim 15 may be grouped with claims 2-5, 16-21, and 23.

VIII. ARGUMENT

A. Is Claim 1 Anticipated by Kameyama?

Claim 1 calls for a method of detecting defective sensing element arrays including reading out a frame of sensing element data from an array and determining the number of defective elements by analyzing said data during the frame readout. Claim 1 is not anticipated by Kameyama, *inter alia*, because Kameyama fails to teach the determination of the number of defective pixels by analyzing the data during the frame readout.

The Applicant has argued that Kameyama fails to teach or suggest the determination of the number of defective elements by analyzing the data during the frame read out. The Examiner responds that "number of defective pixels would be available after the complete frame was read out and analyzed by determining the last space in memory used." But this begs the patentability question. It amounts to an assertion that what the Applicant claims to be doing, could be done in the cited reference, even though the cited reference does not bother to do so. Even if that were

so, it is irrelevant to the anticipation inquiry. The reference does not teach determining the number of pixel elements.

Further, the Examiner argues that "the amount of memory used for a fixed length address, and additional information, would indicate the number of addresses stored and, thus, the number of defective pixels." By the term "indicate," the Examiner obviously means that it would provide information from which the number of pixels could be determined. But, again, the test is not what could be done, but what is done. Here, there is no determination of the number of defective elements.

Therefore, the rejection should be reversed.

B. Is Claim 1 Anticipated by Vincent?

With respect to Vincent, the Examiner now contends that "Vincent inherently discloses the determination of the number of defective pixel elements." However, the location of defective pixels does not amount to a determination of the number of pixels. Just because Vincent could determine it from information he has, does not teach doing so.

Moreover, in order to make out an inherency rejection, the reference must necessarily do what is claimed. Here, there is absolutely no indication whatsoever that even if Vincent could determine the number of defective pixel elements, that he ever does so.

Therefore, the rejection based on Vincent should be reversed.

C. Is Claim 6 Anticipated by Kameyama?

Claim 6 depends from claim 1 and calls for identifying in the focal plane of the pixel array which pixels are defective. As explained on page 21, lines 16-19, defect detection circuits may be located on the same die as the imaging sensor or they may be located on different die "all in the same focal plane."

A large number of pages of Kameyama are cited, but none of them relate to identifying "in the focal plane of the pixel array" which pixels are defective. This could be done in the same die in the focal plane of the pixel array or in another die in a common focal plane.

Therefore, the rejection of claim 6, based on Kameyama, should be reversed.

D. Is Claim 15 Anticipated by Vincent or Kameyama or Obvious Over the Combination of Vincent and Kameyama?

Claim 15 calls for an article storing instructions to programmably set high and low limits for pixel intensity values. During the readout of the pixel intensity values from the array, instructions determine the number of defective pixels by analyzing the pixel data from the imaging array in view of the high and low limits for pixel intensity values.

As pointed out above, Vincent does not teach the determination of the number of defective pixel elements. Therefore, Vincent also cannot teach claim 15.

As pointed out above, Kameyama does not teach the determination of the number of defective pixel elements. Therefore, Kameyama cannot anticipate claim 15.

Concerning the 103 rejection asserting a combination of two references (Vincent and Kameyama) both of which fail to teach the claimed invention, a *prima facie* 103 rejection is not made out.

On the one hand the Examiner contends that claim 15 is anticipated by either Vincent or Kameyama and on the other hand indicates that the same claim is obvious over the combination of the two. Surprisingly, this is not a typographical error. Obviously, one of the Examiner's positions is wrong.

Moreover, there is no rationale to combine Vincent and Kameyama. Since neither teaches the claimed invention, the combination is unavailing.

Therefore, the alternative and inconsistent rejections should be reversed.

IX. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: March 23, 2004

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APPENDIX OF CLAIMS

The claims on appeal are:

1. A method of detecting defective sensing element arrays comprising:

reading out a frame of sensing element data from an array; and

determining the number of defective elements by analyzing said data during the frame read out.

2. The method of claim 1 wherein said sensing element array is an imaging array, said method further including programmably setting high and low limits for pixel intensity values.

3. The method of claim 2 further including programmably setting said high and low limits based on illumination conditions.

4. The method of claim 2 further including comparing the pixel intensity values measured by said array to said high and low limits.

5. The method of claim 4 further including indicating a defect when a pixel's intensity value is higher than said high limit or lower than said low limit.

6. The method of claim 1 wherein said sensing element array is an imaging array, said method further including identifying in the focal plane of the pixel array, which pixels are defective.

7. The method of claim 1 wherein said sensing element array is an imaging array and said data is pixel data, said method further including determining the number of spatial defects by analyzing said pixel data in said imaging array.

8. The method of claim 7 including determining whether two defective pixels are closer together than a programmable offset.

9. The method of claim 8 further including adding a column or row address where a defect exists to a programmable offset and storing said address with said offset.

10. The method of claim 9 further including comparing the address of a defective pixel to said stored address plus a programmable offset.

11. The method of claim 1 further including identifying the number of spatial defects by column and row by analyzing, in said array, said data.

12. The method of claim 1 further including storing information about the location of defective elements in a memory in said array.

13. The method of claim 12 wherein each element in the array has a corresponding location in the memory and setting a defect exists bit at each memory location where a defective element has been identified.

15. An article comprising a medium that stores instructions that cause a processor-based system to:

programmably set high and low limits for pixel intensity values; and

determine during the read out of pixel intensity values from the array, the number of defective pixels by analyzing pixel data from said imaging array in view of said high and low limits for pixel intensity values.

16. The article of claim 15 further storing instructions that cause a processor-based system to programmably set said high and low limits based on illumination conditions.

17. The article of claim 15 further storing instructions that cause a processor-based system to compare the pixel intensity values measured by said array to said high and low limits.

18. The article of claim 15 further storing instructions that cause a processor-based system to determine the number of spatial defects by analyzing said pixel data in said imaging array.

19. The article of claim 18 further storing instructions that cause a processor-based system to determine whether two defective pixels are closer than a programmable offset.

20. The article of claim 15 further storing instructions that cause a processor-based system to identify the number of spatial defects by column and row by analyzing said pixel data.

21. The article of claim 15 further storing instructions that cause a processor-based system to store information in a memory about the location of a defective pixel.

22. A sensing device comprising:

a plurality of sensing elements capable of indicating information to be captured; and

a circuit in said device adapted to determine the number of defective elements by analyzing the element data as it is read out from said elements.

23. The device of claim 22 wherein said device is an imaging device and said elements are pixels, said device including storage adapted to enable high and low limits for pixel intensity values to be set programmably.

24. The device of claim 22 further including a circuit adapted to determine the number of spatial defects by analyzing data as it is read out from said elements.

25. The device of claim 24 further including a window circuit that is adapted to add a column or row address where a defect exists to a programmable offset and to store said address with said offset.

26. The device of claim 25 further including a comparator adapted to compare the address of a defective element to the stored address plus the programmable offset.

27. The device of claim 22 further including a memory adapted to store information about the location of defective elements.

28. The device of claim 27 wherein said memory includes a location corresponding to each of a plurality of elements.

29. The device of claim 22 wherein said circuit and said elements are formed on the same die.

30. The device of claim 22 wherein said device is an imaging device and said elements are pixels, said circuit being formed on the imaging device's focal plane that includes said pixels.